electrically connecting said selected ones of the plurality of conductive pads to the plurality of contacts.

I3 Concluded

REMARKS

The Examiner has suggested a new title. The title has been amended accordingly.

The Office Action devotes an entire page to reminders of the proper content, language and format for an abstract, but does not raise any objections to, or make any comments about, the existing abstract. Applicants maintain that the abstract in its current form fully meets all the requirements for an abstract.

Claims 19, 21 and 26 have been rejected under 35 USC 112(1) for containing a negative limitation in claim 19 that is not in the original disclosure (i.e., "not coupling a microprocessor device . . . testing"). Claim 19 has been amended accordingly.

Claims 19, 21 and 26 have been rejected under 35 USC 112(2) as being indefinite for failing to particularly point out and distinctly claim the subject matter. To explain the intent of the rejection, the Office action then asks the following questions, which are followed by Applicants' answers.

1) *How does the passing or failing of the cache memory affect the microprocessor device?* It only affects whether the microprocessor and the cache memory will be

joined into a common assembly. Any other effect on the microprocessor is outside the scope of the claim.

2) *Is the mircroprocessor device mounted on the interposer and then to a substrate or to a substrate alone*? It does not matter. It only matters that the cache memory is tested before such coupling, so that the decision of whether or not to couple the microprocessor and cache memory together may be made, based on the results of the test. This temporal relationship is clearly defined in claim 19 by the 'if-then' phrasing of the claim.

3) *If the testing does not affect the microprocessor device, what prevents mounting of the processor on the substrate*? This limitation was erroneous and has been amended to state that the microprocessor device is not coupled to the interposer if the testing fails. Since the term 'coupled' may indicate either a direct or indirect (i.e., through other devices) connection, the claim states that if the testing fails, the microprocessor device will not be connected directly or indirectly to the interposer (and thus to the cache memory).

4) *Is the testing performed on the microprocessor and the substrate*? The only testing claimed is on the cache memory devices, and that must be performed before the microprocessor and/or substrate are coupled to the interposer/cache memory devices. Any testing that might be performed on the microprocessor and/or substrate is outside the scope of the claims.

Claims 19, 21 and 26 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent no. 5,635,847 ("Seidel") in view of U.S. patent no. 5,483,421 ("Gedney")

and further in view of U.S patent no. 5,680,936 ("Beers) and U.S. patent no. 5,983,490 ("Sakemi"). Applicants respectfully traverse these rejections because the cited references do not disclose or suggest every element of any claim, as the following analysis shows.

Independent claim 19 recites that the non-selected conductive pads, that is, the conductive pads that do not receive solder bumps, are non-selected because they are not intended to be used. Support for this limitation may be found in the specification at page 9 lines 8-9. Sakemi, which has been cited to provide the limitation of non-selected locations, does not disclose or suggest this limitation. The non-selected pads of Sakemi are non-selected only because they are defective. This is stated in numerous places in Sakemi, including the abstract and in col. 2 lines 12-17. Sakemi further shows that the non-selected locations were intended to be used, because they would not be tested for defects (col. 2 line 13-14) if there was no intention to use them.

Claims 21 and 26 depend from claim 19 and therefore contain the same limitations not disclosed or suggested by the cited references.

CONCLUSION

For the foregoing reasons, Applicants submit that claims 19, 21 and 26 are now in condition for allowance, and indication of allowance by the Examiner is respectfully requested. Applicants further submit that claims 22, 24 and 25 should now be considered and found allowable in view of the allowance of claims 19, 21 and 26. If the Examiner has any questions concerning this application, he or she is requested to telephone the undersigned

at the telephone number shown below as soon as possible. No fee is believed due in connection with this amendment. In this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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APPENDIX A

MARKED-UP COPY OF TITLE

[TESTING A MULTI-CHIP INTERPOSER]

METHOD OF ASSEMBLING A MULTI-CHIP DEVICE

MARKED-UP COPY OF AMENDED CLAIMS

19. (Amended nine times) A method of assembling a multi-chip device comprising:

populating a second surface of an interposer having a first surface and the second surface with a plurality of conductive pads;

coupling solder balls to selected ones of the plurality of conductive pads;

not coupling the solder balls to non-selected ones of the plurality of conductive pads, said non-selection being based on intended non-use of the non-selected ones;

coupling a plurality of cache memory devices and at least one passive device to the first surface to form a multi-chip subassembly, wherein the at least one passive device is selected from a group consisting of resistors, capacitors, and inductors;

testing said plurality of cache memory devices on said interposer;

coupling said interposer to a substrate with the solder balls and coupling a microprocessor to the substrate after said testing if said plurality of cache memory devices pass said testing; and

not coupling said interposer to the substrate and not coupling [a] the microprocessor device to the interposer [substrate] if said plurality of cache memory devices does not pass said testing.